Highly Integrated Gradient Pulse Generator for Magnetic Resonance Imaging System

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ABSTRACT: A gradient pulse generator for magnetic resonance imaging is presented. It has the ability to yield arbitrary gradient pulses on the fly and provide reconfigurable calculations including scaling, axis rotation, pre-emphasis, and gradient offsetting in real time along *X, Y,* and *Z* gradient channels. The versatility has been obtained by incorporating all required digital functions into a single field programmable gate array chip. The development of the hardware is eased by employing a high-level tool—the System Generator—using the MathWorks model-based Simulink environment. In addition, an easy-to-use method is developed for pre-emphasis calibration. As expected, the described device is highly integrated, low cost, simple to use and interface, and has been demonstrated successfully in conjunction with a home-built magnetic resonance system to perform imaging experiments. © 2011 Wiley Periodicals, Inc. Concepts Magn Reson Part B (Magn Reson Engineering) 39B: 59–63, 2011

KEY WORDS: magnetic resonance imaging; gradient pulse generator; preemphasis; field programmable gate array

I. INTRODUCTION

In magnetic resonance imaging (MRI), the magnetic field gradients are necessary to spatially encode the object into MR signals, sensitize the image contrast to motion, selectively choose or edit MR signals, and minimize image artifacts (*1*). As a unit of an MR spectrometer, a gradient pulse generator creates and controls gradient signals before they are fed into a gradient amplifier. As MR has ability to acquire images in any plane, the gradient orientation should be controlled in real time along the *X*, *Y*, and *Z* gradient channels (*2*). The pre-emphasis is also required to alter the gradient pulse shape for compensating the induced eddy currents (*3–6*).

Several designs reported in the previous literature separate the pre-emphasis unit with the gradient controller (*7–11*). As many electronic components and printed circuit boards are needed, the circuit complexity increases, and the costs are expensive. The pre-emphasis constants are set in the form of discrete elements or controlled by potentiometers (*9*, *10*), which are hard to adjust and program. Recently, in designs of some standard MR spectrometers, dedicated digital signal processor (DSP) is often employed for gradient pulse generation and calculations (*12*, *13*). However, these designs still seem complex (multiple DSPs are utilized together on one or several circuit boards); as a result, the apparatuses are hard-to-develop, and the costs are relatively high. Herein, we propose a highly integrated gradient pulse generator based on a single field programmable gate array (FPGA) chip. As a compact and low-cost (less than $200) module, it is not only capable of control-

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Table 1 Main Characteristics of the Gradient Pulse Generator

Characteristics	Attributes
Circuit board dimension	10×22 cm^2
Waveform memory	$32{,}000 \times 32$ bit
Rotation matrix	1K 3×3 matrices (32-bit word length)
Pre-emphasis	32-Bit programmable constants; four set constants per gradient channel
Analog output	± 10 V differential for X, Y, and Z channels; 24-bit DAC
Minimum pulse length	0.96 μs

ling on-the-fly gradient pulse generation but also providing real time calculations required for gradient scaling, axis rotation, and pre-emphasis. The device is under control of a pulse programmer to communicate with a MR spectrometer. Its main characteristics have been summarized in Table 1.

FPGA has been known for its inherent parallelism, reconfigurability, and flexible interface. These advantages make FPGA become mainstream in designing digital circuits. However, it is often uneasy to manipulate traditional FPGA designs, because the register transfer level (RTL) developments using hardware description language (HDL) is complex and time consuming. The idea behind the project is to simplify the design of a gradient pulse generator upon a high-level platform, which provides both system modeling and automatic code generation for the developers without much FPGA experience. In this work, the System Generator, one of Xilinx's DSP design tools (ISE design suite 12.3, Xilinx, San Jose, CA), is fully used. The tool integrates RTL, embedded, intellectual property (IP) core, and hardware resources for design entry in the MathWorks model-based Simulink environment (Matlab R2009a, MathWorks, Natick, MA). Apart from automatic code generation, it also supports hardware validation, resource estimation, and power analysis (*14*). This article aims to mainly describe the function and principle of the system design and experiment demonstrations of the presented device. Some implementation details such as modeling sources are left out, as they are available to the scientific community by corresponding author's e-mail.

II. SYSTEM DESIGN

The block diagram of the circuit is shown in Fig. 1. An FPGA (XC3SD1800A, Xilinx) performs all functions needed for gradient pulse generation and calculations. The digital gradient pulses along X, Y, and Z channels are then converted into analog signals through three audio DACs (PCM1704, Texas Instruments, Dallas, TX).

Five main logic blocks are implemented inside the FPGA, including a signal processing unit, a dual-port block random-access memory (RAM), a register file, a digital clock manager (DCM), and a temperature monitor. The 32-bit parallel port can be used for programming and reading register values, communicating with a pulse programmer (TMS320C6413, Texas Instruments) through an external memory interface (EMIF). The DCM provides a system clock of 100 MHz for synchronous processing and a bit clock of 25 MHz for DACs. The register file contains 48

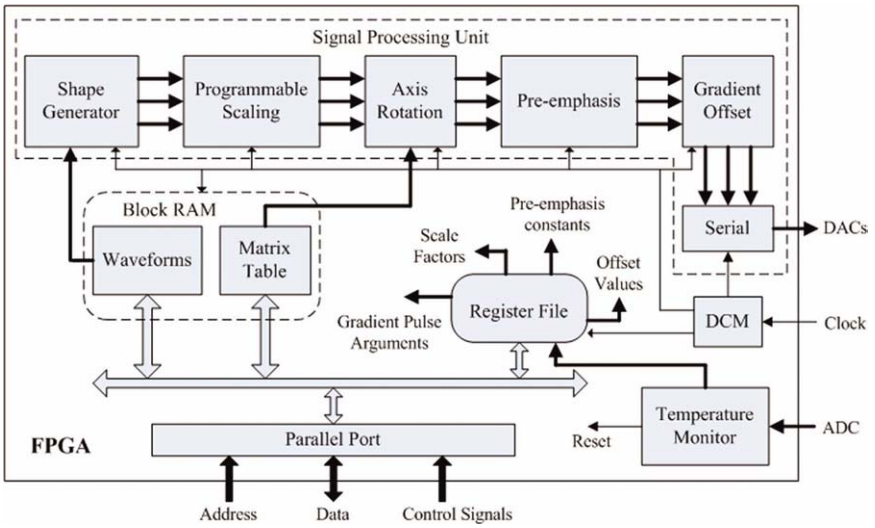

Figure 1 Block diagram of the gradient pulse generator based upon a single FPGA.

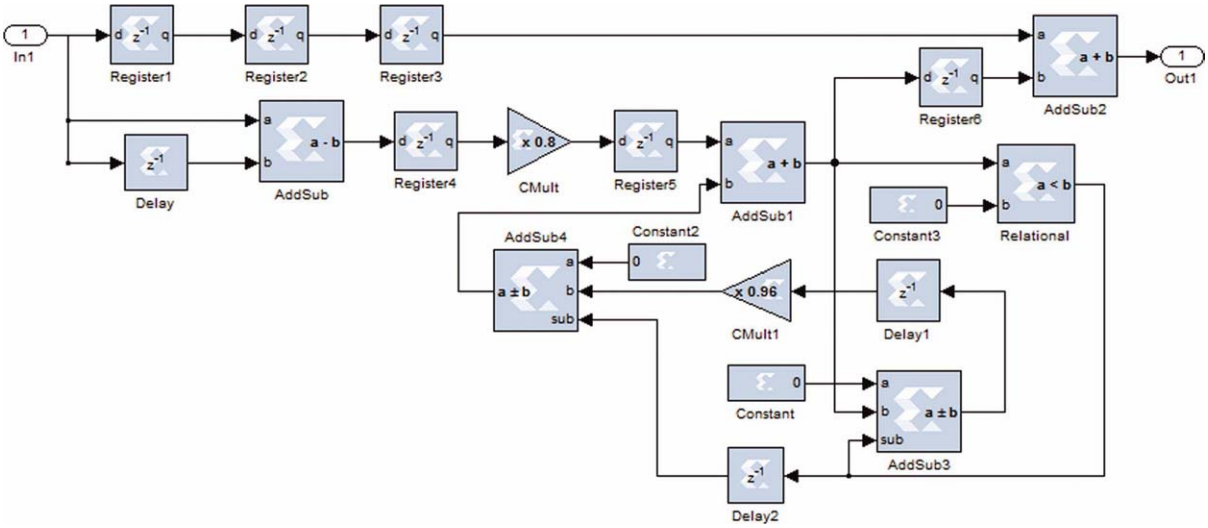

Figure 2 Implementation diagram of preemphasis calculation with one time and amplitude constant. The HDL code can be automatically generated from the diagram using the System Generator.

32-bit registers implemented in a fast distributed RAM. There are three types of registers in the file, including control, data, and status registers. The control register reads an instruction word, which is sent by the pulse programmer and used to produce trigger signals for waveform generation. The data register is used as a data buffer of programmable parameters such as gradient pulse arguments, amplitude scale factors, preemphasis constants, and gradient offset values. A status word in the status register reflects the rounding errors of gradient calculations as well as the result from the temperature monitor. The monitor reads a multichannel ADC (MAX1167, MAXIM, Sunnyvale, CA) to acquire temperature signals of the sensors on gradient coils. If any measured signal exceeds predefined value, it will automatically reset all three gradient outputs to zero and inform the host PC. The block RAM consists of two parts: one is for the storage of base relative gradient waveforms, and the other for rotation matrices. The values inside the RAM are initiated by the pulse programmer. A maximum waveform memory depth of 32,000 and up to 1,024 rotation matrixes are allowed during one pulse sequence.

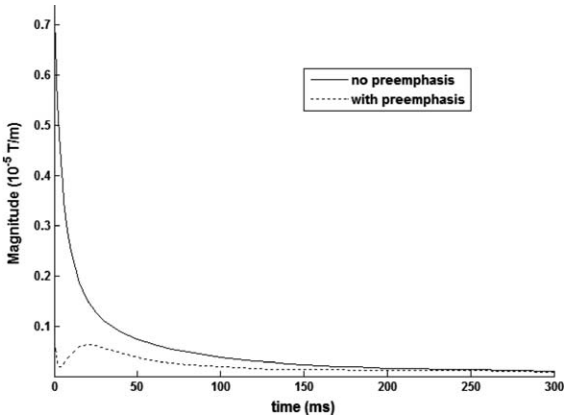

Figure 3 The result of eddy currents generated by X gradient with no preemphasis compensation (solid line), and with preemphasis compensation (dashed line).

For each of gradient channels, the signal processing unit is divided into six operation blocks using three pipeline stages. The total pipeline latency is less than 300 system clocks, allowing for a short delay of approximately 3 μs relative to the requested time origin of a gradient event. The shape generation, scale multiplication, and axis rotation are accomplished sequentially during the first pipeline stage; the pre-emphasis calculation and gradient offsets setting during the second pipeline stage; the last stage contains parallel to serial conversion for output data. The sampling period of gradient pulses is determined by the execution time for the slowest pipeline stage. It is programmable, ranging from 0.96 μs (equivalent to the period of parallel to serial data conversion) to approximately 100 μs in multiples of 10 ns. Once a gradient event is triggered, the shape generator reads out 32-bit base relative amplitude of the pulse per sampling period according to gradient arguments, and holds the final value constant until another event commences. The gradient arguments include the starting address of the shaped pulse, the pulse length, and the sampling period. Any new arguments can be written to associated shadow registers at any time during a sampling period. The contents in shadow registers become active only when a certain gradient event occurs. This double buffering feature allows

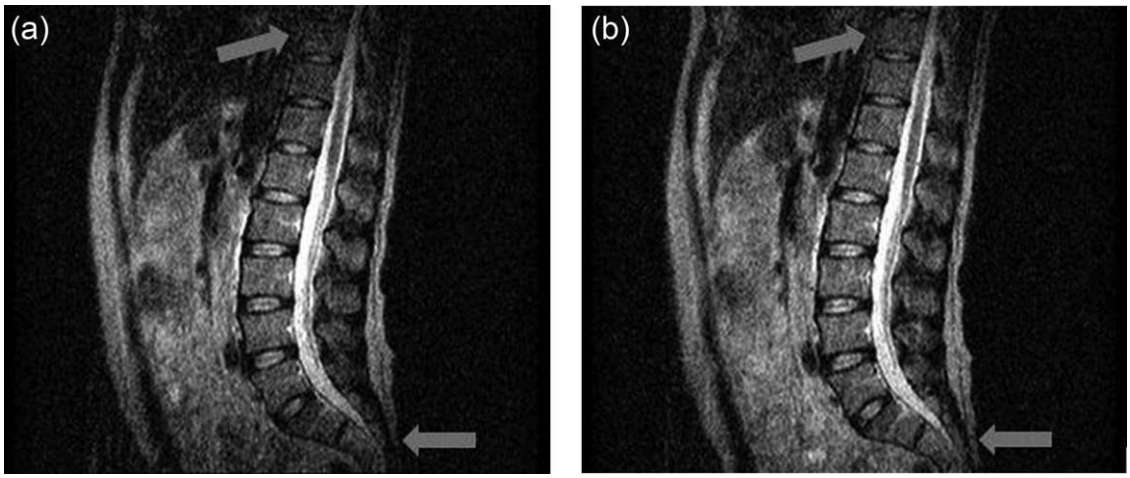

Figure 4 Sagittal T_2-weighted images of a volunteer's lumbar spine obtained with FSE sequence in a 0.36 T permanent magnetic system. The experiments arguments are as follows: spectrometer frequency (SF) = 15.3 MHz, repetition time (TR) = 3,100 ms, echo time (TE) = 138 ms, slice thickness =5 mm, FOV = 350 × 314 mm^2, acquisition matrix = 256 × 235. (a) Uncompensated pre-emphasis and (b) fully compensated pre-emphasis using the proposed method.

updating a gradient pulse on the fly to change the gradient arguments for the sampling period that follows. The amplitude is then multiplied by the programmable scale factor, enabling flexible adjustment of slice thickness, phase encoding increment, and field of view (FOV) in two dimensions without rewriting pulses. The scaled results are referred to as logical waveforms. They are converted into the waveforms along the physical axes when oblique imaging is required. In axis rotation, the logical waveforms are multiplied by a predefined 3 × 3 orthogonal rotation matrix which describes a translation in three-dimensional space.

The values resulting from matrix multiplication are then passed to the second pipeline stage to perform pre-emphasis. To compensate eddy currents induced from time-varying magnetic fields, it is necessary to tailor physical waveforms into specific overdrive shapes. According to inductive-resistive (LR) circuit model (*3*, *4*), eddy-current impulse response is given by a sum of decaying exponentials characterized by time and amplitude constants, respectively. In digital domain, the compensated pulse $g[n]$ is given by the equation listed below:

$$\begin{aligned} g[n] &= x[n] + \sum_{i=1}^{m} y_i[n] \\ &= x[n] + \sum_{i=1}^{m} \alpha_i (x[n] - x[n-1]) \\ &\quad + \beta_i y_i[n-1], \quad \beta_i = e^{-\omega_i} \end{aligned} \qquad [1]$$

where $x[n]$ is uncompensated pulse and the second term is sum of multiexponential functions with characteristic time constants $1/\omega_i$ and amplitude constants α_i. In our system, four independent exponential overdrives (i.e., taking $m = 4$ in Eq. [1]) are adequate because of the utilization of shielded gradient coils. For simplicity, Fig. 2 shows an implementation diagram of preemphasis calculation with one time and amplitude constant using the system generator. It is noted that the intermediate negative term (i.e., $y_i[n-1] < 0$ in Eq. [1]) is inverted before multiplied by the exponential multiplicand, and then restored to the original value after multiplication. This step ensures that there is no significant quantization error in the exponential multiplication that could lead to imperfect preemphasis result. After pre-emphasis, the gradient pulses are added by predefined offsets, facilitating gradient shimming in a digital manner. The execution period for this pipeline stage is fixed as 0.96 μs. When an overflow occurs in gradient calculations, a flag will be set as error in the status register and the result is automatically saturated to the maximum value.

The final function is to generate serial bit stream of gradient pulse for digital to analog conversion. A 32-bit word is first truncated into a 24-bit data and then serially shifted out with the bit clock from DCM. The maximum bit clock rate for PCM1704 is 25 MHz; therefore, the execution period for this stage is 0.96 μs.

III. EXPERIMENT RESULT

We incorporated the described gradient pulse generator into a home-built permanent MRI system (~0.36 T) to

demonstrate its performance. Although actively shielded gradient coils are used, preemphasis is yet necessary to minimize the effect of eddy currents. For pre-emphasis setting, a calibration procedure is developed to determine optimum constants in eddy-current compensation. First, we run the pulse sequence proposed by Vincent J S et al. (*6*) with all pre-emphasis constants set to zero. After acquiring the uncompensated eddy currents, we use a fitting tool (Curve Fitting Tool, MathWorks, Inc., Natick, MA) to estimate initial values of time and amplitude constants. Then we set these values into the gradient pulse generator and keep the time constants unchanged in the remaining procedure. Subsequent measurements are obtained with varied amplitude constants but maintaining the proportional relationship between each other. The iteration may be continued by repeating the above steps until the root mean square (RMS) value of measured eddy currents is minimum. Figure 3 shows the result of uncompensated eddy currents in *X* channel and the corresponding result of compensated eddy currents with four sets of constants found using the described method. The strength of eddy currents with pre-emphasis has been reduced to a value less than 0.7 μT/m. In *Y* and *Z* channels, the values of eddy current strengths are even lower.

Figure 4 compares two sagittal T_2-weighted images of a volunteer's lumbar spine using fast spin echo (FSE) sequence. The signal loss is manifest at the top and the bottom where the gray arrows point out in Fig. 4(a), which is acquired with no pre-emphasis. As expected, in Fig. 4(b) acquired using fully compensated preemphasis, the signal loss is much reduced.

IV. CONCLUSION

A highly integrated gradient pulse generator is described in this article. The device, based on a single FPGA chip, is versatile in terms of arbitrary waveform generation, amplitude scaling, oblique imaging, preemphasis, and gradient offsetting. The system generator, a high-level tool based on the Simulink environment, simplifies the development of the hardware design. In addition, an easy-to-use pre-emphasis adjustment method is presented to facilitate eddy-current compensation with up to four sets of programmable constants. The gradient pulse generator has advantages of compactness, low cost, and flexibility and is successfully in use with a home-built MRI spectrometer.

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