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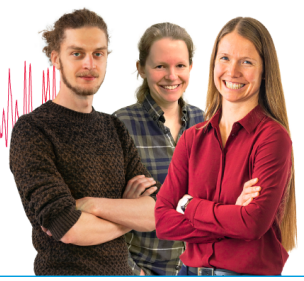

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# Quiescent power consumption of carbon-based analog operational amplifiers at low temperatures

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## ABSTRACT

In modern integrated circuit systems, quiescent power consumption increases with higher integration density, posing a fundamental limitation for further integration scaling. This challenge becomes even more critical in cryogenic environments, such as superconducting quantum computing and space exploration applications, where ultralow quiescent power consumption is essential for maintaining reliable circuit operation at extremely low temperatures. Using the unique low-temperature electrical properties of carbon nanotube materials, we fabricated a carbon nanotube field-effect transistor (CNT-FET) that exhibits significantly reduced currents under cryogenic conditions. These carbon-based FETs were implemented to construct a carbon nanotube analog operating amplifier (CNT-OPA). Comprehensive experimental characterization across a wide temperature range (293–10 K) revealed that the CNT-OPA's quiescent power consumption decreases at cryogenic temperatures without any degradation in the gain performance. These results demonstrate the strong potential of carbon-based analog amplifiers for cryogenic electronic applications, particularly in superconducting quantum computing systems and space electronics where conventional silicon-based devices face fundamental limitations.





Driven by the unique properties and application demands of cryogenic electronics, various cryoelectronic devices have been developed in recent years. Cryogenic environments offer several advantages, including reduced thermal noise, enhanced carrier mobility, and the ability to observe and exploit quantum effects in electronic devices; these benefits are critical for applications such as superconducting quantum computing, which require robust cryoelectronic support systems.[1–3] Driven by continuous advancements in fields like artificial intelligence and quantum computing, the demand for computational power is constantly increasing, placing higher requirements on circuit integration. However, escalating integration levels exacerbate the issue of chip power consumption, particularly in high-integration scenarios where quiescent power consumption sometimes approaches dynamic power consumption levels. For a long time, silicon-based chip technology advanced under the guidance of Dennard scaling, according to which as device dimensions (W, L; W represents channel width, L represents channel length) decreased, the operating voltage ($V_{dd}$) and threshold voltage ($V_t$) would scale proportionally, keeping the electric

field in the channel constant. As a result, the dynamic power density $[V_{dd} \times I_{on}/(W \times L)]$ remained unchanged. However, when silicon-based technology reached the 90 nm process node (with a physical gate length of 40–50 nm), the quiescent power consumption of chips increased dramatically due to the exponential growth in transistor count, approaching the level of dynamic power. Further increase in the chip's operating frequency led to higher total power density, generating more heat. Once the heat exceeded the chip's cooling capacity, the temperature would rise continuously, causing performance degradation or even thermal failure. The most effective way to reduce power density is to lower the operating voltage. However, in conventional silicon-based transistors, switching is governed by thermionic emission, and the Boltzmann distribution of electrons imposes a fundamental limit: the subthreshold swing (SS) cannot be less than 60 mV/dec at room temperature. To maintain both a low off-state current ($I_{off}$) and a high on-state current ($I_{on}$), the operating voltage cannot be scaled down effectively. Consequently, further increases in operating frequency had to be sacrificed in order to keep the chip's power density within thermal limits.[4]

When Si CMOS circuits operate at low temperatures, variabilities and other degradation effects caused by incomplete dopant ionization due to low injection doping, carrier freeze out, and undesirable kink effects can lead to circuit failure.[5,6] Additionally, other issues arise in low temperature environments: an increase in the semiconductor material's bandgap due to the disappearance of significant thermal diffusion; the emergence of quantum effects;[7,8] a decline in the impedance matching performance of passive components; and an increased need for 1/f noise management due to reduced thermal noise.[2,8–10] Typically, chips are placed within a temperature range of 3–4 K to achieve a higher power budget, which sets the upper limit for chip power consumption.[11] To enhance carrier transport capabilities, it is often necessary to increase operating voltage.[12,13] Some silicon-based amplifiers, while claiming operational capability at 4 K temperatures, actually require active heating to maintain elevated temperatures (e.g., above 130 K) for proper functioning.[13] This heating requirement would compromise the cryogenic environment in applications where maintaining low temperatures is essential. Another type of semiconductor device based on gallium nitride (GaN) material, high-electron-mobility transistors (HEMTs), exhibits good performance at liquid helium temperatures, but it suffers from the "kink effect" under low-temperature conditions.[14]

In contrast to silicon-based devices, carbon-based devices, particularly carbon nanotube (CNT) devices, owing to their non-doping process and the excellent physical properties of carbon nanotubes, demonstrate superior electrical and physical characteristics at low temperatures.[15] Carbon nanotube materials offer a range of physical advantages over silicon-based materials.[16–20] Carbon-based devices are significantly less susceptible to carrier freeze out effects at low temperatures compared to their silicon counterparts.[21] Their unique band structure and potential for one-dimensional ballistic transport are more readily realized at cryogenic temperatures, offering the prospect of breaking the Boltzmann limit to achieve lower subthreshold swing (SS) and higher operating frequencies.[15,22] Although carbon-based materials have been around for quite some time, their physical and electrical properties remain an active area of exploration.[23] Meanwhile, other research teams are working to directly fabricate electronic devices from these materials to validate and demonstrate their potential;[20,24–27] these efforts include the design and development of carbon-based electronic devices,[16,17,28] study of carbon-based devices with high temperature stability,[16,24] system-level validation,[25] and 3D integration initiatives.[29–31] From the perspective of environmental protection and sustainable development, some research teams have developed devices using carbon nanotube materials that achieve a high recovery rate, showing promise in mitigating the potential accumulation of environmentally and biologically toxic materials from electronic waste in the future.[32] In addition to exploring and demonstrating specific theories and technologies related to carbon-based electronics, several research groups also contribute systematic articles summarizing advancements in this field. This allows us to stay updated on the key developments and challenges in the field of carbon-based electronics, including the lack of high-throughput analytical methods for detecting ultralow concentrations of metallic CNTs, the need for a scalable and sustainable manufacturing approach to produce sufficient quantities of ultrahigh-purity semiconducting CNTs, determining the most appropriate combination of materials and processes; and realizing high-quality and scalable contacts for n-type CNT transistors.[33] However, there have been only few reports on carbon-based operational analog amplifiers to date. Here, we present a carbon-based operational amplifier developed by our team. This carbon-based operational amplifier (CNT-OPA) maintains normal operation across a wide temperature range from 293 to 10 K without requiring adjustment of its supply voltage. Unlike conventional commercial silicon-based amplifiers, this carbon-based amplifier operates normally at cryogenic temperatures without requiring active self-heating to specific temperatures, thereby preserving cryogenic environmental integrity while ensuring reliable functionality. Most importantly, this carbon-based amplifier achieves a significant reduction in quiescent power consumption at low temperatures without compromising dynamic gain.

The unpackaged CNT-OPAs were characterized using a cryogenic probe station system maintained by a multi-stage dry cryocooler and vacuum pumps. The probe station consists of six probe arms as shown in Fig. 1(a), corresponding to the six pins of our carbon-based amplifier. The sample stage is operated with microscope assistance. The chip is fixed on the sample stage surface using vacuum grease while maintaining good thermal contact between the chip and stage, as illustrated in Fig. 1(b). Device characterization was performed using a Keithley 4200B semiconductor analyzer and Keysight B2902B source meter, enabling comprehensive assessment of

- carbon nanotube field-effect transistor (CNT FET) transfer/output characteristics;
- carbon-based OPA output curves;
- quiescent power consumption metrics across temperature conditions.

The structural schematic diagram of the CNT FET is shown in Fig. 2(a), while the scanning electron microscopy (SEM) image is presented in Fig. 2(b). The CNT FETs were fabricated using a local bottom-gate structure on 100 mm silicon wafers with 285 nm thermal oxide.[34] The key process steps include the following:

(1) Gate electrode formation, which involved deposition of lithographically patterned Ti/Au (1 nm/30 nm) gates via electron-beam evaporation.
(2) High-$\kappa$ dielectric stack, which involved atomic layer deposition (ALD) of $Y_2O_3$/Hf $O_2$/$Y_2O_3$ trilayers at 200 °C, with $Y_2O_3$

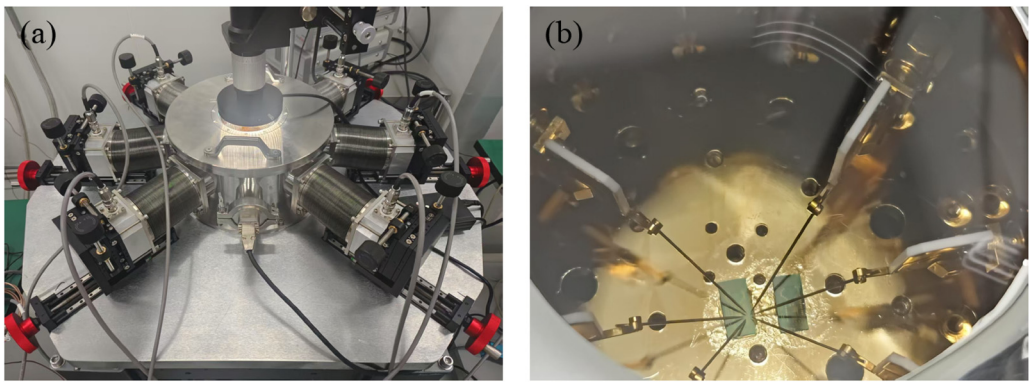


**FIG. 1.** (a) Image of cryogenic probe station; and (b) close-up image of probe-to-chip interface.

interlayers formed by Y metal evaporation (3 nm) followed by thermal oxidation (250 °C, 15 min air ambient).

(3) Contact engineering, which involved wet etching (diluted HCl) and reactive-ion etching (RIE) to define dielectric openings.
(4) CNT channel integration, which involved transfer-processed semiconducting CNT films patterned via lithography and oxygen plasma RIE.
(5) Metallization, which involved deposition of Ti/Pd/Au (0.5 nm/20 nm/20 nm) source/drain contacts by e-beam evaporation and liftoff.
(6) Passivation and doping:

- PMOS: dual-layer $Y_2O_3$ passivation (2 × evaporated/oxidized Y).
- NMOS: AlN electrostatic doping via plasma-enhanced ALD (250 °C), with PMOS regions protected by tetramethylammonium hydroxide (TMAH) wet etching.

The CNT-OPA comprises nine carbon-based field-effect transistors. Its architecture can be divided into three distinct sections, as shown in Fig. 3(a). These carbon-based MOSFETs exhibit nonuniform gate lengths, with their scanning electron microscopy (SEM) images presented in Fig. 3(b). The two-stage operational amplifier (OPA) architecture consists of three main parts: a differential input stage, a gain stage, and a bias network. The first stage is a differential input structure formed by transistors M1–M5, responsible for signal comparison; the second stage is a common-source amplifier (M6–M7) that provides voltage gain. The bias network employs a Wilson current mirror structure (M8–M9), which supplies stable bias currents to the circuit. Furthermore, the width-to-length (W/L) ratios of all transistors were optimized as core design parameters.

During DC characteristic testing, the carbon-based amplifier was fixed on a stable probe test platform with a stable power supply of ±1 V applied to its positive and negative terminals. The current mirror control voltage was adjusted individually for each amplifier to ensure maximum gain and output range. Static power consumption was recorded after continuous operation for over one hour. For the DC input-output characterization, the negative input terminal was

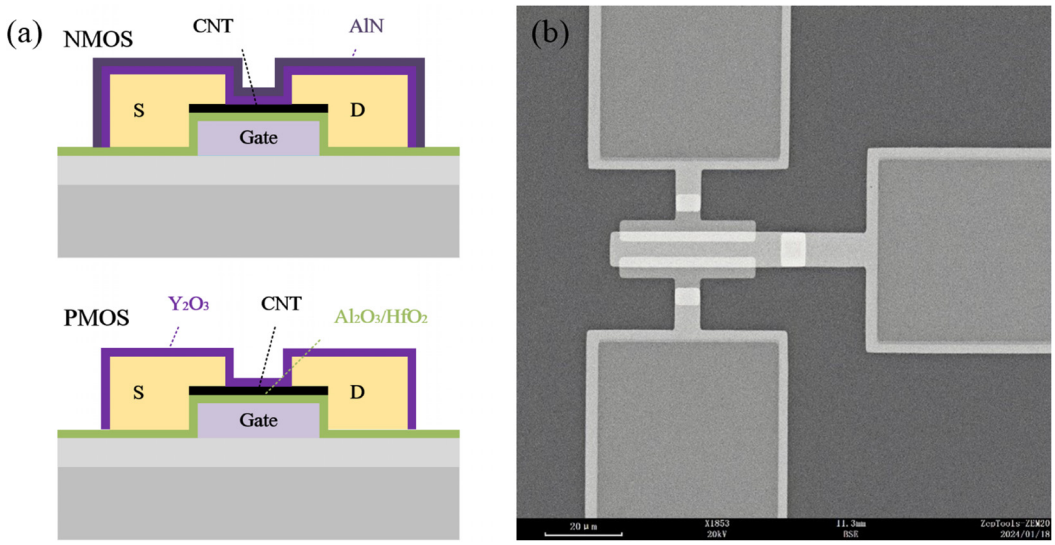


**FIG. 2.** (a) Schematic diagram of the CNT MOSFET. (b) Microscopy image of the CNT MOSFET.

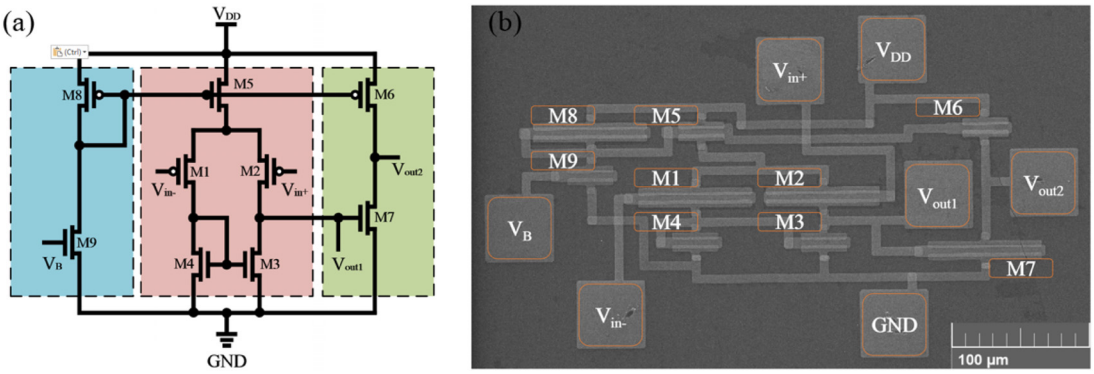


**FIG. 3.** (a) Schematic diagram of the CNT-OPA. (b) Microscopy image of the CNT-OPA.

grounded (0 V), while the positive input terminal was swept from −1 V to +1 V.

The quiescent power consumption of an operational amplifier is primarily determined by its constituent field-effect transistors (FETs). Therefore, device-level characterization of the constituent carbon-FETs was performed before functional verification of the CNT-OPA. We start by comparing the electrical performance of the FETs comprising the OPA at 293 K and under several low-temperature conditions, with a particular focus on their current characteristics. We tested MOS transistors, measuring transfer and output characteristic curves at different temperatures. To better visualize the current magnitudes at these temperatures, the transfer characteristic curves in this section are plotted using logarithmic axes. Figure 4(a) shows the drain current at 10 K (solid lines) vs 293 K (dashed lines), with different colors representing distinct gate voltages. For identical drain and gate voltages, the drain current is consistently lower at 10 K. As the data are plotted on a logarithmic scale, the reduction in drain current at 10 K relative to 293 K remains within one order of magnitude across all measured conditions. For this CNT-MOS sample, we calculated and plotted key parameters across varying temperatures in Fig. 4(b). The quiescent current (measured at $V_{DS} = V_{GS} = 1$ V, $V_S = 0$, triangular data points) decreases with reducing temperature—consistent with the behavior in Fig. 4(a)—confirming drain current reduction at cryogenic conditions under identical bias. The subthreshold swing (SS, circular data points) shows monotonic improvement (decrease) with cooling, while the maximum transconductance ($g_{m,max}$, square data points) increases at low temperatures. This collectively indicates superior performance of the CNT-OPA at cryogenic temperatures.

We characterized the input–output response of five CNT-OPAs at 293 K, with test results shown in Fig. 5(a). All amplifiers demonstrate normal functionality, exhibiting linear amplification behavior near the zero-input bias point. Subsequently, we measured the gain of these amplifiers across varying temperatures. The normalized results in Fig. 5(b) show no consistent trend in gain variation with temperature reduction. The gain of an OPA depends on multiple parameters, such as transistor transconductance ($g_m$), output resistance ($r_o$), and threshold voltage ($V_{th}$). In practical operation, individual transistors also experience operational voltage fluctuations, unlike the controlled conditions used for maximum $g_m$ testing. Consequently, the gain behavior across temperatures does not follow the consistent trend observed with maximum transistor transconductance. However, our experimental data show that the OPA gain maintains uncompromised performance at low temperatures. Next, we measured the current magnitudes of the positive and negative current sources under no-load

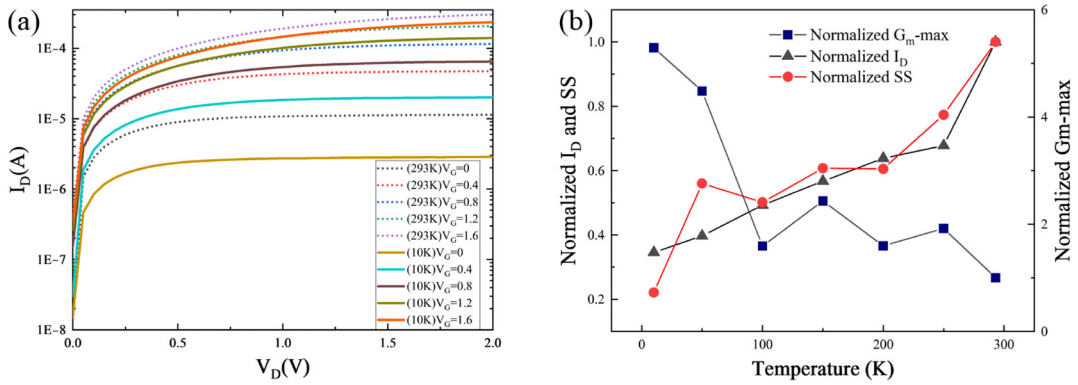


**FIG. 4.** (a) The transfer characteristic curve of an CNT-NMOS transistor at 293 K (showed in dashed line) and at 10 K (solid line). (b) The relationships of $I_D$ (drain current), SS (subthreshold swing), and $G_m$ (max transconductance) with different temperature.

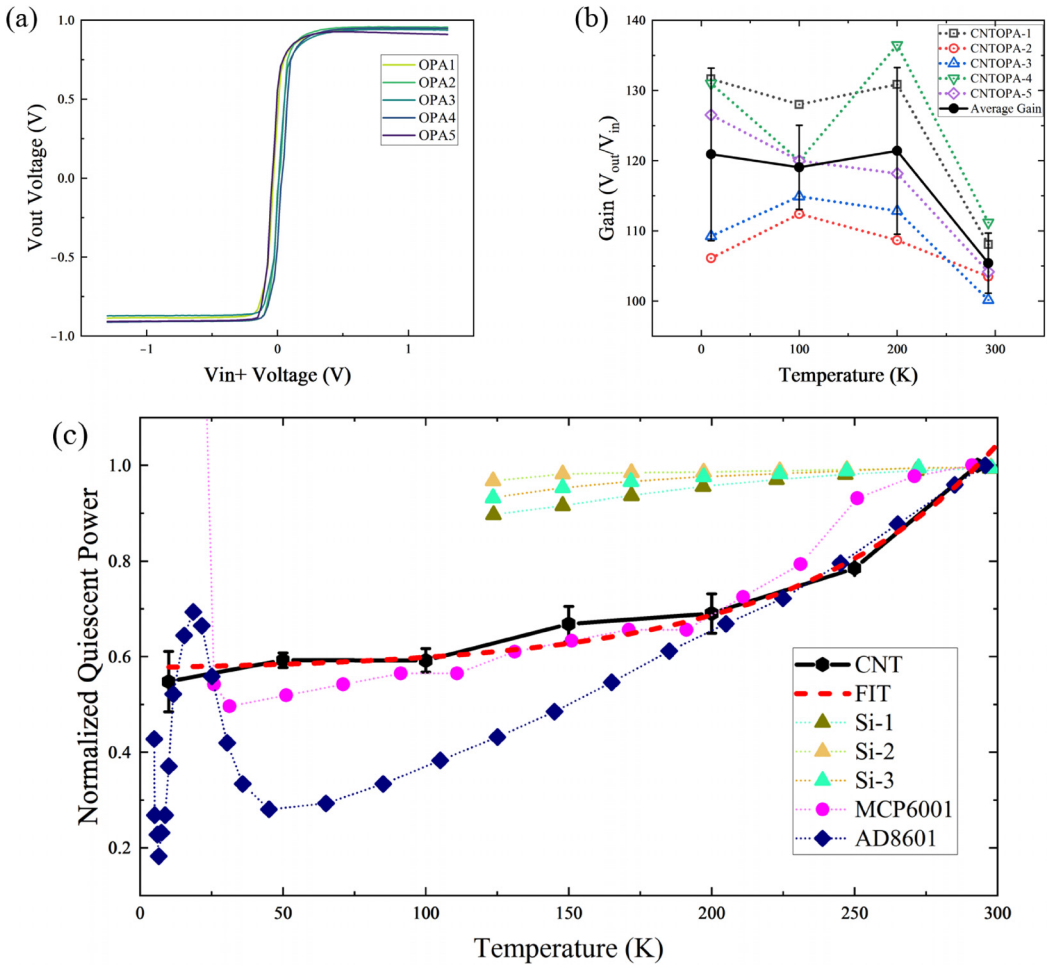


**FIG. 5.** Test results of carbon-based OPA. (a) Output characteristics of the operational amplifiers with the positive input scanned from −1.5 to 1.5 V while the negative input was grounded. (b) Gain vs temperature characteristics for these carbon-based operational amplifiers. (c) Comparison of normalized quiescent power consumption vs temperature for carbon-based operational amplifiers, a silicon-based operational amplifier,[35] and commercial references (MCP6001 and AD8601).[13] A dashed trendline is fitted to the carbon-based amplifier data.

conditions (but remains $V_B = 0$ V). The quiescent power consumption $P_Q$ is proportional to both the supply voltage $V_{DD}$ and leakage current $I_{leak}$,

$$P_Q = V_{DD} \cdot I_{leak+} + V_{GND} \cdot I_{leak-}, \quad (1)$$

where $V_{DD} = +1$ V, $V_{GND} = -1$ V, and $I_{leak}$ corresponds to the measured currents from the positive and negative supplies. In summary, we present the quiescent power consumption of the CNT-OPAs measured across varying temperatures, with normalized results shown in Fig. 5(c), including a trend fit line for temperature dependence. The figure incorporates quiescent power consumption data from both a conventional silicon-based OPA[35] and a test result of MCP6001 and AD8601,[13] enabling direct comparison with the carbon-based OPA's quiescent power characteristics. Although Ref. 14 contains quiescent power data for multiple operational amplifiers, we have excluded data from amplifiers exhibiting analogous characteristics, as well as those requiring active self-heating to achieve operational temperatures, due to concerns that such heating mechanisms could compromise cryogenic environmental integrity. Through comparative analysis, it can be observed that as the ambient temperature decreases, the quiescent power consumption of our CNT-OPA exhibits a systematic reduction.

The fitting results of quiescent power consumption vs temperature obey the relation

$$QP = 0.43e^{0.014(T-293)} + 0.57. \quad (2)$$

The fitting model uses nonlinear curve fitting (based on an exponential growth model with offset), yielding an R-squared ($R^2$) value of 0.9787. This curve approximately reflects the relationship between the quiescent power consumption of this batch of carbon-based OPAs and their operating ambient temperature.

Although transistor off-state currents exhibit temperature dependence,[17] precise quantitative prediction of the amplifier's quiescent power across temperature ranges remains challenging due

to operational variations among constituent transistors and their varying degrees of cutoff. Consequently, based on experimental results, we advance this tentative hypothesis.

Observation of this single-trend fitting curve reveals discrepancies in the fitting accuracy, particularly for data at 10 K. Combining theoretical analysis, we re-examined the temperature dependence of quiescent power consumption. In the high-temperature regime (>150 K), the dominant mechanism in carbon-based materials involves phonon scattering dynamics. The mobility ($\mu$) follows a power-law relationship with temperature (T),

$$\mu \propto T^{-\gamma} \quad \text{where} \quad \gamma = 1\text{–}2. \tag{3}$$

For CNT, $\gamma = 1.5$, thus

$$\mu_{\text{CNT}} \propto T^{-1.5} \quad (\text{1D confined scattering}). \tag{4}$$

The corresponding electrical resistance expression is given by

$$R \propto T^{\gamma}. \tag{5}$$

The exponential term in quiescent power ($P_{\text{quiescent}}$) is essentially an approximation for phonon scattering,

$$P_{\text{quiescent}} \propto \frac{1}{\mu} \propto T^{\gamma} \approx e^{\gamma \ln T}. \tag{6}$$

In the 293–150 K temperature range, $\ln T$ exhibits near-linear behavior, reducing the equation to

$$e^{\gamma \ln T} \rightarrow e^{b(T-293)} \quad \text{with} \quad b = 0.014. \tag{7}$$

The coefficient $b$ is theoretically calculated as follows:

$$\begin{aligned} b &= \gamma \cdot (\ln T)T \\ &= 1.5 \times \frac{1}{T}\bigg|_{T=293} \\ &= 1.5 \times \frac{1}{293} \\ &\approx 0.00512 \quad (\text{vs experimental value } 0.014). \end{aligned} \tag{8}$$

We hypothesize that in carbon-based materials at high temperatures, whether due to electron–plasmon coupling or other related mechanisms, the actual temperature exponent $\gamma$ exceeds theoretical predictions.

Below 100 K, as temperature continues to decrease, carbon nanotubes exhibit phonon freezing and progressively transition to ballistic transport, representing a distinct transport regime fundamentally different from the mechanisms dominating above 150 K. So the sub-100 K data trend violates the high-temperature (>150 K) model, causing substantial deviations in fitting accuracy, most notably at the 10 K measurement point.

Figure 5(c) reveals that the quiescent power consumption of silicon-based amplifiers (Si-1 to Si-3, open hexagons) and GeSi amplifier (open triangles) decreases moderately with temperature reduction. However, their reduction magnitude is significantly smaller than our CNT-OPA (solid hexagons) at equivalent temperatures. In particular, previous studies lack sub-100 K data for these conventional amplifiers, likely due to cryogenic malfunction or experimental limitations. AD8601 (navy blue open diamonds) shows superior power reduction above 50 K compared to CNT-OPA but exhibits fluctuations and an upward trend below 50 K. MCP6001 (light magenta open diamonds) exhibits monotonic reduction down to 30 K (comparable to CNT-OPA), followed by a sharp increase below this threshold. At deep cryogenic temperatures (not shown), its power consumption increases to more than 13 times the value measured at 293 K.

Notably, our carbon-based amplifier operates at a constant voltage across all temperature conditions. Effective thermal exchange with the baseplate is ensured through thermal grease application, and the temperature measurement point corresponds precisely to the baseplate temperature. This configuration confirms that the amplifier's operational temperature equals the documented ambient temperature.

While certain conventional carbon-based amplifiers fail to function in the 4 K regime without modifications—like Microchip MlC860 and Analog Devices AD8605 and AD8651, which need different power supply settings for proper operation—they can achieve operability through specific adjustments, such as increasing operating voltage or elevating the amplifier's own temperature (e.g., TLC271 requires self-heating to 130 K for proper operation).[13] However, such active heating measures to raise the amplifier's temperature may potentially compromise the integrity of the cryogenic environment.

The test results show that the CNT-OPA exhibits reduced quiescent current consumption at low temperatures without compromising dynamic gain. This indicates that the reduction in quiescent power consumption does not come at the expense of the amplifier's gain. Throughout the test, the carbon-based OPA's supply voltage was held constant (symmetric ±1 V power supplies). In contrast to conventional OPAs (where carrier freeze out necessitates higher voltages at low temperatures), these carbon-based OPAs maintain operation without additional power requirements. Based on the test results above, when the temperature decreases to 10 K, the quiescent power consumption of this carbon-based operational amplifier is reduced to below 60% of its value at 293 K. The CNT-OPA integrates transistors with heterogeneous channel lengths, as shown in Fig. 3(b). Under practical working conditions, each transistor exhibits operational variations, which differ from the controlled voltage applied during individual transistor off-state current testing. Consequently, the proportional reduction in the amplifier's overall quiescent power with temperature deviates from the off-current reduction ratio observed in standalone transistor measurements.

In summary, we demonstrate a carbon-based FET and its integration into a carbon-based OPA. The chips maintained normal operation across a broad temperature range from room temperature (293 K) down to cryogenic conditions (10 K), exhibiting excellent temperature adaptability. Unlike certain conventional OPAs as mentioned above that require elevated operating voltages to function properly under cryogenic conditions,[13] this CNT-OPA operates without voltage adjustment. Moreover, its quiescent power performance improves with decreasing temperature. At 10 K, the quiescent power consumption decreases to approximately 54.8% of its 293 K value. The quiescent power follows an approximately exponential decay trend as the temperature decreases. These results indicate that the carbon-based OPA holds great promise for applications requiring both wide-temperature-range adaptability and low power consumption, such as quantum bit (qubit) readout and signal processing in superconducting quantum computing, as well as other extreme cryogenic environments.

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## AUTHOR DECLARATIONS

### Conflict of Interest

The authors have no conflicts to disclose.

### Author Contributions

Zhe Liu and Haojin Xiu contributed equally to this work.

**Zhe Liu:** Data curation (equal); Investigation (equal); Validation (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal). **Haojin Xiu:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (lead); Resources (equal). **Nan Wei:** Conceptualization (lead); Methodology (equal); Resources (lead); Supervision (equal); Writing – review & editing (equal). **Chunwei Wang:** Investigation (equal); Writing – original draft (equal); Writing – review & editing (equal). **Haipeng Wang:** Conceptualization (equal); Resources (equal); Writing – review & editing (equal). **Ningfei Gao:** Conceptualization (equal); Methodology (equal); Resources (equal). **Haitao Xu:** Conceptualization (equal); Methodology (equal); Resources (equal). **Xiaoji Zhou:** Conceptualization (equal); Funding acquisition (lead); Project administration (lead); Resources (equal); Supervision (lead); Writing – review & editing (equal).

## DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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